AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 2, line 19, and ending at page 2, line 28, as follows:

Figure 1 is a block diagram illustrating a precision timing component or a clock signal synchronization system 101 in accordance with the present invention. By way of example, Fig. 1 shows system 101 is a part of a universal serial bus (USB) device 100 and functions for ~~generate~~ generating a clock signal synchronized with a packet received from a host (not shown in Fig. 1) via a USB bus 110. In Fig. 1 an element 102 represents portions of USB device 100 other than clock signal synchronization system 101. Element 102, which is also referred to as a data processing element, may include a USB control circuit and other components of USB device 100. The USB control circuit, which is sometimes also referred to as a USB driver, functions to control the data transfer between the host and an external or slave device, e.g., USB device 100, via USB bus 110.

Please amend the paragraph beginning at page 2, line 29, and ending at page 3, line 9, as follows:

USB device 100 can be any kind of ~~devices~~ device that communicates with a host via USB bus 110. Examples of USB device 100 include, but are not limited to, USB mouse for moving a cursor on the host computer screen and making commands to the host computer, USB memory device (e.g., USB hard drive, USB CD-ROM, USB rewritable CD, USB rewritable DVD, USB flash memory, etc.), USB multimedia devices (e.g., USB CD player, USB DVD player, USB MP3 player, etc.). USB bus 110 is

coupled between USB device 100 and the host or master device. As well known in the art, USB bus 110 includes four wires or lines, two of which are data transmission (D+) line 112 and complementary data transmission (D-) line 114, and the other two are power supply line 115[[,]] and ground line 117. In accordance with an embodiment of the present invention, clock signal synchronization system 101 is fabricated on an integrated circuit chip that realizes part or whole functions of USB device 100.

Please amend the paragraph beginning at page 5, line 6, and ending at page 5, line 28, as follows:

After detecting the incoming packet, data sequence analyzer 104 seeks to identify the type of the packet in a step 304. Specifically, data sequence analyzer 104 verifies whether the incoming packet is a token packet in step 304. In a specific embodiment of the present invention, data sequence analyzer 104 identifies the incoming packet as a token packet in response to the packet satisfying three preset conditions. The first condition is a time duration or interval between the first falling edge (edge 202 in Fig. 2) and the second rising edge (edge 203 in Fig. 2) being approximately equal to a time duration or interval between edge 203 and the second falling edge (edge 204) in wave 210 ~~represents~~ <u>representing</u> the voltage level at the D+ line. The second condition is a time duration between the first falling edge (edge 202) and the second falling edge (edge 204) being approximately equal to a time duration between edge 204 and the third falling edge (edge 206) in wave 210. The third condition is a time duration between the first falling edge (edge 202) and the third falling edge (edge 206) being approximately equal to a time duration between edge 206 and

the fourth falling edge (edge 208) in wave 210. In accordance with the present invention, any timing signal can be used to measure the time durations. For example, in a preferred embodiment of the present invention, the reference frequency signal from RC oscillator 103 is used for the time measurement. Generally speaking, the higher the frequency of the reference frequency signal [[is]], the more accurate the time measurement will be. In accordance with a preferred embodiment, two time durations are considered to be approximately equal to each other if a difference there between is less than about ten percent (10%). In accordance with another preferred embodiment, two time durations are considered to be approximately equal to each other if a difference there between is less than about five percent (5%). Other criteria are within the spirit of the present invention and also fall into the scope of the present invention.

Please amend the paragraph beginning at page 7, line 11, and ending at page 7, line 24, as follows:

At the beginning of each cycle of the reference signal of RC oscillator 103, process 400, in step 403, checks the signal level at element 102 to see whether USB device 100 is receiving or waiting for a packet from the host. ~~IfUSB~~ If USB device 100 is receiving or waiting for packets [[for]] from the host, process 400 detects whether there is a change in the voltage level at the D+ or D- line in USB bus 110. The change in the voltage level while USB device is receiving a data stream from the host indicates a change in the bit value of the incoming data stream. The detected bit may be a bit in the token packet or in any other packets following the token packet in the data stream. In response to detecting [[the]] a change in the voltage level, process 400 generates a

start edge, e.g., a rising edge, for a cycle of the synchronized clock signal in a step 404. Therefore, the start edge of the current cycle in the clock signal is synchronized or locked to the beginning of a bit period in the incoming packet. After generating the start edge of the synchronized clock signal in step 404, process 400 returns to step 402 with counters 106 and 108 reset to zero. Process 400 is ready for the next cycle.

Please amend the paragraph beginning at page 7, line 25 and ending at page 8, line 3 of the Specification as follows:

No change in the voltage level indicates there is no change in the bit value. This may correspond to two situations. The first situation is that the time lapse from the previous cycle of process 400 is not equal to the time duration of one or more bits in the incoming packet because consecutive bits in the incoming packet may have the same bit value. The second situation is that USB device 100 is sending an outgoing data stream to the host. In response thereto, the counts of counters 106 and 108 increase by one [[a]] at step 406. In a subsequent step 407, process 400 checks whether the count C_{106} of counter 106 satisifies Equation (1):

$$\cancel{C_{106} = /J_{>>}xiV/8} \quad \underline{C_{106} = D \times N / 8} \tag{1}$$

In equation (1), D is the value of the digital control signal generated in process 300 described herein above with reference to Fig. 3, and N is a positive integer.